

DESIGN OF LOW POWER HIGH PERFORMANCE 16-POINT 2-PARALLEL PIPELINED FFT ARCHITECTURE

SENTHIL SIVAKUMAR M & BANUPRIYA M & AROCKIA JAYADHAS S

Faculty in St.Joseph University, Tanzania

ABSTRACT

In this paper, we proposed a low power high performance 16-point 2-parallel pipelined FFT architecture with the use of various low power functional block implementation techniques. This paper presents the techniques to minimize the power consumption of the FFT architecture by reducing number of functional blocks used to implement the FFT processor. The FFT is employed by the modified radix-4 algorithm to significantly reduce the number of complex multipliers. The parallel pipelined technique is introduced to increase the throughput of the circuit at low frequency. The IDR commutator technique is used to reduce the power dissipation by reducing the total elements used for the memory element compare to conventional commutator. Multiplier is a foremost device which increases the size of real-time FFT processors. In this paper, we replaced such complex multipliers by minimum number of adders and shifters with two's complement and canonical signed-digit (CSD) representations. Also the new low power butterfly architecture is introduced to implementing the radix-4 butterfly operation that reduces the area and power consumption of the FFT processor. The employments of these low power techniques in 16-point FFT architecture is yield 45% of power minimization compare to the conventional FFT architecture. The output values are achieved by the simulation and synthesis of Verilog HDL codes in cadence RTL compiler using tsmc18_wl10.

KEYWORDS: Butterfly Architecture, CSD, FFT, Low Power, Parallel and Pipelined Fftarchitecture, R4SDC FFT.